

Claims

We claim:

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is defined as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member, wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

4. The electronic structure of claim 1, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

1 5. The electronic structure of claim 1, wherein the solder member includes a controlled collapse
2 chip connection (C4) solder ball.

1 6. The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

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1 7. An electronic structure, comprising:

2 a semiconductor substrate having a first electrically conductive pad thereon;

3 an organic substrate having a second electrically conductive pad thereon, wherein a
4 surface area of the first pad exceeds a surface area of the second pad;

5 a solder member electrically coupling the first pad to the second pad; and

6 an underfill material between the semiconductor substrate and the organic substrate,
7 wherein the underfill material encapsulates the solder member, and wherein the underfill material
8 has an elastic modulus of at least about 1 gigapascal.

1 8. An electronic structure, comprising:

2 a semiconductor chip having a first electrically conductive pad thereon;

3 an organic chip carrier having a second electrically conductive pad thereon, wherein a
4 surface area of the first pad exceeds a surface area of the second pad;

5 a solder member electrically coupling the first pad to the second pad; and

6 an underfill material between the semiconductor chip and the organic chip carrier,

7 wherein the underfill material encapsulates the solder member, and wherein the underfill material

8 has an elastic modulus of at least about 1 gigapascal.

1 9. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon, wherein a
4 surface area of the first pad exceeds a surface area of the second pad by a factor of at least about
5 1.2; and
6 a solder member electrically coupling the first pad to the second pad.

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1 10. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon, wherein a
4 surface area of the first pad exceeds a surface area of the second pad by a factor between about
5 1.1 and about 1.3; and
6 a solder member electrically coupling the first pad to the second pad.

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1 11. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon, wherein a
4 surface area of the first pad exceeds a surface area of the second pad by a factor between about
5 1.3 and about 2.0; and
6 a solder member electrically coupling the first pad to the second pad.

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1 12. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon; and
4 a solder member electrically coupling the first pad to the second pad, wherein a
5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm.

1 13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the
2 organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

1 14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P
2 is defined as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder
3 member, wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the
4 semiconductor substrate.

1 15. The electronic structure of claim 12, wherein the organic substrate includes an organic
2 material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene,
3 and combinations thereof.

1 16. The electronic structure of claim 12, wherein the solder member includes a controlled
2 collapse chip connection (C4) solder ball.

1 17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

[illegible]

1 18. An electronic structure, comprising:

2 a semiconductor chip having a first electrically conductive pad thereon;

3 an organic chip carrier having a second electrically conductive pad thereon;

4 a solder member electrically coupling the first pad to the second pad, wherein a
5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and

7 an underfill material between the semiconductor chip and the organic chip carrier,

8 wherein the underfill material encapsulates the solder member, and wherein the underfill material
9 has an elastic modulus of at least about 1 gigapascal.

1 19. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon;
4 a solder member electrically coupling the first pad to the second pad, wherein a
5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and
7 an underfill material between the semiconductor substrate and the organic substrate,
8 wherein the underfill material encapsulates the solder member, and wherein the underfill material
9 has an elastic modulus of at least about 1 gigapascal.

1 20. An electronic structure, comprising:
2 a semiconductor substrate having a first electrically conductive pad thereon;
3 an organic substrate having a second electrically conductive pad thereon; and
4 a solder member electrically coupling the first pad to the second pad, wherein a
5 distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.40 mm.

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1 21. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad; and
5 electrically coupling, by use of a solder member, the first pad to the second pad.

1 22. The method of claim 21, wherein a coefficient of thermal expansion (CTE) of the organic
2 substrate is between about 10 ppm/°C and about 18 ppm/°C.

1 23. The method of claim 21, wherein P is between about .15 and about .75, wherein P is defined
2 as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member,
3 wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the
4 semiconductor substrate.

1 24. The method of claim 21, wherein the organic substrate includes an organic material selected
2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations
3 thereof.

1 25. The method of claim 21, wherein the solder member includes a controlled collapse chip
2 connection (C4) solder ball.

1 27. A method of forming an electronic structure, comprising:
2 forming a semiconductor chip having a first electrically conductive pad thereon;
3 forming an organic chip carrier having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad;
5 electrically coupling, by use of a solder member, the first pad to the second pad; and
6 placing an underfill material between the semiconductor chip and the organic chip carrier,
7 wherein the underfill material encapsulates the solder member, and wherein the underfill material
8 has an elastic modulus of at least about 1 gigapascal.

1 28. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad;
5 electrically coupling, by use of a solder member, the first pad to the second pad; and
6 placing an underfill material between the semiconductor substrate and the organic
7 substrate, wherein the underfill material encapsulates the solder member, and wherein the
8 underfill material has an elastic modulus of at least about 1 gigapascal.

1 29. A method of forming an structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at
5 least about 1.2; and
6 electrically coupling, by use of a solder member, the first pad to the second pad.

1 30. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor
5 between about 1.1 and about 1.3; and
6 electrically coupling, by use of a solder member, the first pad to the second pad.

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1 31. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon,
4 wherein a surface area of the first pad exceeds a surface area of the second pad by a factor
5 between about 1.3 and about 2.0; and
6 electrically coupling, by use of a solder member, the first pad to the second pad.

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1 32. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon; and
4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm.

1 33. The method of claim 32, wherein a coefficient of thermal expansion (CTE) of the organic
2 substrate is between about 10 ppm/°C and about 18 ppm/°C.

1 34. The method of claim 32, wherein P is between about .15 and about .75, wherein P is defined
2 as $(C_{\text{SOLDER}} - C_{\text{ORGANIC}})/(C_{\text{SOLDER}} - C_{\text{SEMI}})$, wherein C_{SOLDER} is a CTE of the solder member,
3 wherein C_{ORGANIC} is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the
4 semiconductor substrate.

1 35. The method of claim 32, wherein the organic substrate includes an organic material selected
2 from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations
3 thereof.

1 36. The method of claim 32, wherein the solder member includes a controlled collapse chip
2 connection (C4) solder ball.

1 37. The method of claim 32, wherein the solder member includes a lead-tin alloy.

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1 38. A method of forming an electronic structure, comprising:

2 forming a semiconductor chip having a first electrically conductive pad thereon;

3 forming an organic chip carrier having a second electrically conductive pad thereon;

4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and

7 placing an underfill material between the semiconductor chip and the organic chip carrier,
8 wherein the underfill material encapsulates the solder member, and wherein the underfill material
9 has an elastic modulus of at least about 1 gigapascal.

1 39. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon;
4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.25 mm; and
7 placing an underfill material between the semiconductor substrate and the organic
8 substrate, wherein the underfill material encapsulates the solder member, and wherein the
9 underfill material has an elastic modulus of at least about 1 gigapascal.

1 40. A method of forming an electronic structure, comprising:
2 forming a semiconductor substrate having a first electrically conductive pad thereon;
3 forming an organic substrate having a second electrically conductive pad thereon; and
4 electrically coupling, by use of a solder member, the first pad to the second pad, wherein
5 a distance from a centerline of the solder member to a closest lateral edge of the semiconductor
6 substrate is at least about 0.40 mm.

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